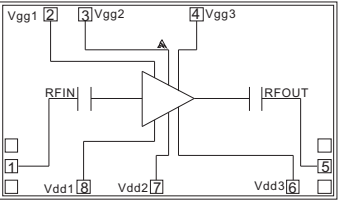


性能特点

- 工作频率：8.0~12.0GHz
- 饱和输出功率：29dBm @ PIN = 8dBm
- 功率附加效率：30% @ PIN = 8dBm
- 小信号增益：23dB @ Vdd = +8V，
- 功率增益：21dB @ PIN = 8dBm
- 偏置条件：Vdd = +8V，Idq = 210mA，Vgg = -0.6V(典型值)
- 输入/输出阻抗：50Ω
- 芯片尺寸：2.65mmx1.53mmx0.10mm

功能框图



概述

BW222是一款工作于8.0~12.0GHz的GaAs单片集成功率放大器芯片，在+8V工作电压下，可提供21dB功率增益和29dBm饱和输出功率，功率附加效率30%。

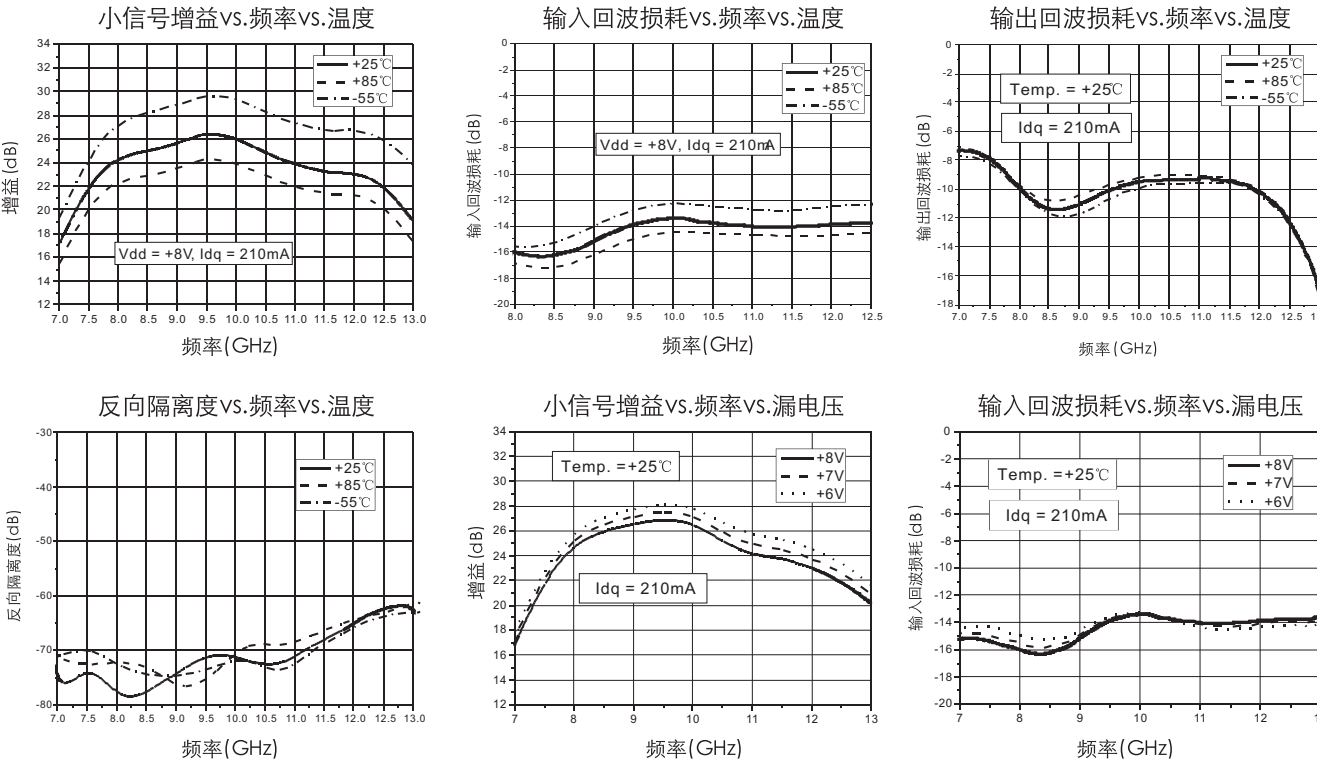
该芯片采用了片上通孔金属化工艺保证良好接地，不需要额外的接地措施，使用简单方便。芯片背面进行了金属化处理，适用于共晶烧结工艺。

电性能表 (TA = +25℃，50Ω system，Vdd = +8V，Idq = 210mA，Vgg = -0.6V(典型值))

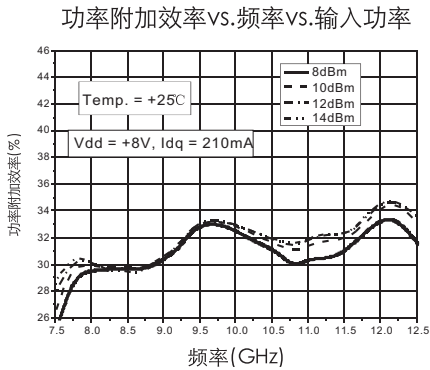
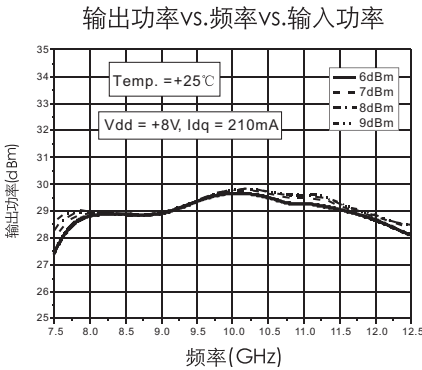
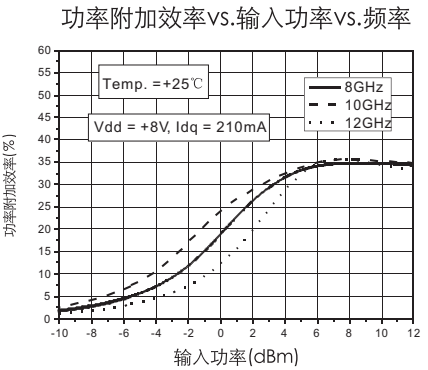
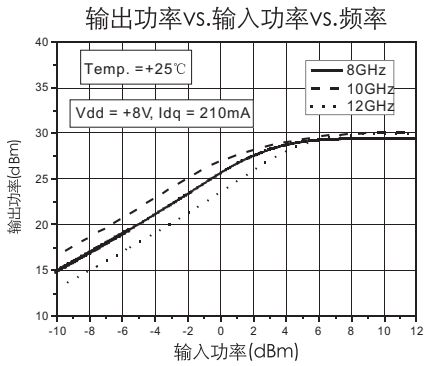
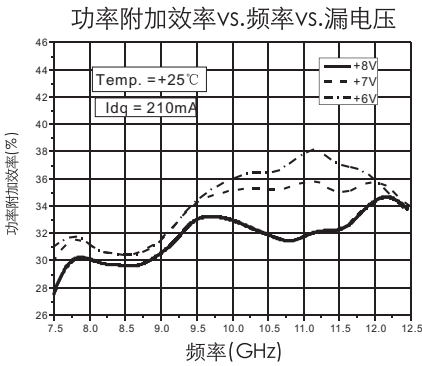
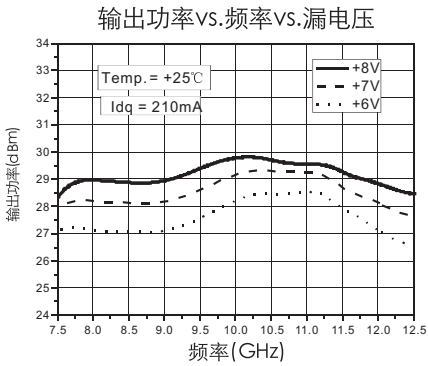
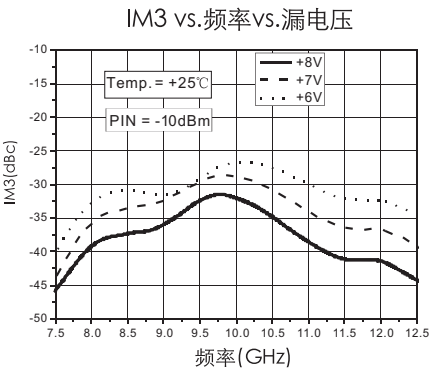
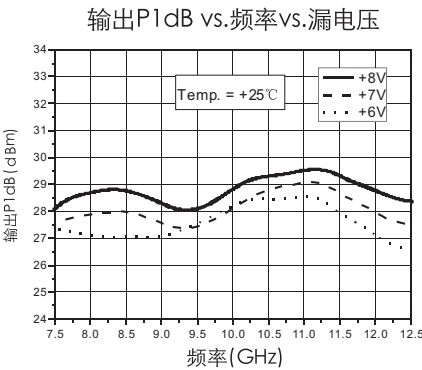
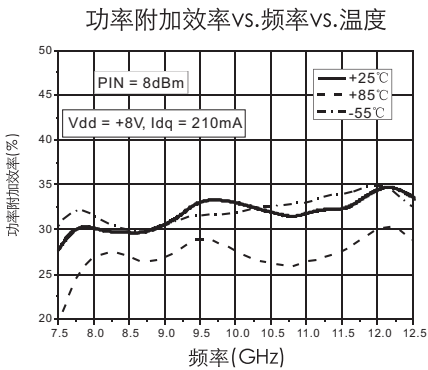
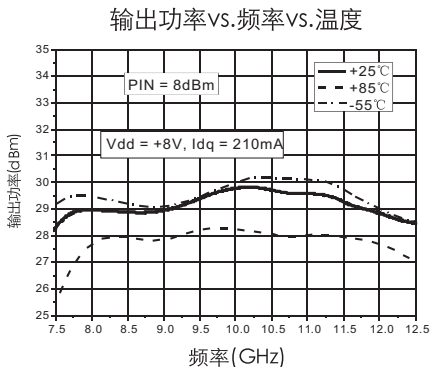
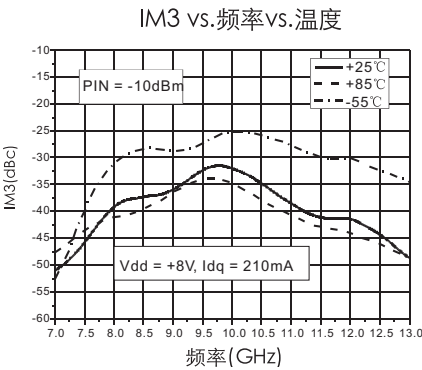
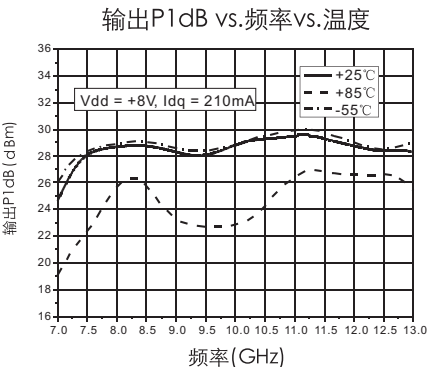
符号	参数名称	最小值	典型值	最大值	单位
Frequency	工作频率	8.0~12.0			GHz
Gain	小信号增益	-	23	-	dB
Gp	功率增益(PIN = 8dBm)	-	21	-	dB
IRL	输入回波损耗	-	8	-	dB
ORL	输出回波损耗	-	10	-	dB
Pout	输出功率(PIN = 8dBm)	-	36	-	dBm
PAE	功率附加效率(PIN = 8dBm)	-	25	-	%
Idd	饱和漏电流(PIN = 8dBm)	-	0.3	-	A

- [1] 芯片均经过在片100%直流与RF测试。
- [2] 在-1.0V与-0.4V之间调整栅压Vgg，使静态漏电流Idq=210mA。

测试曲线(连续波)

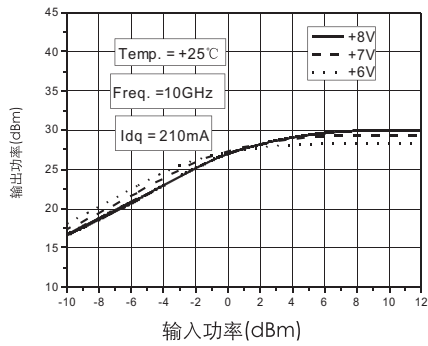


BW222型GaAs单片集成功率放大器

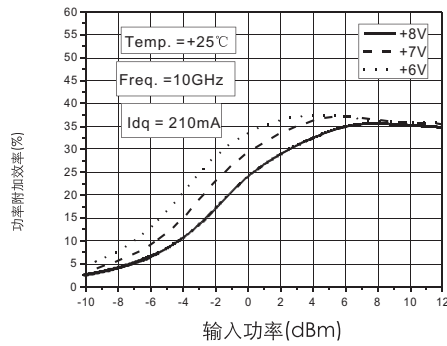


BW222型GaAs单片集成功率放大器

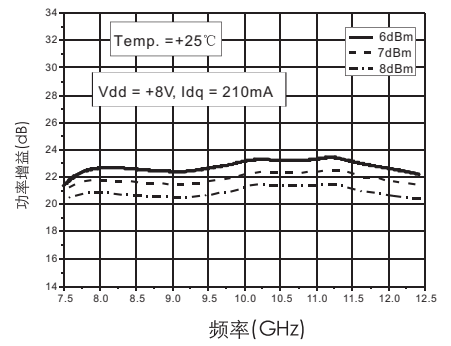
输出功率vs.输入功率vs.漏电压



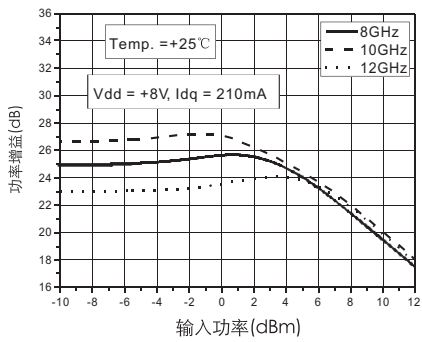
功率附加效率vs.输入功率vs.漏电压



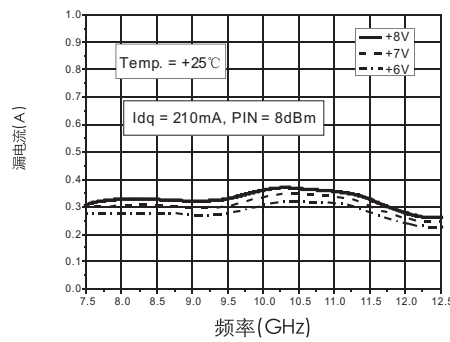
功率增益vs.频率vs.输入功率



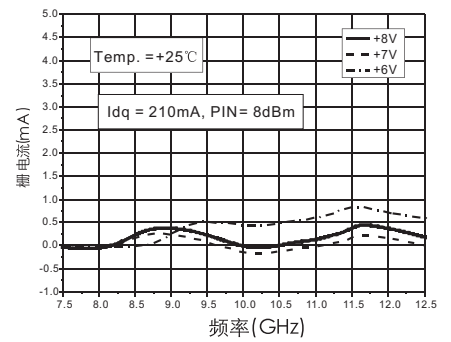
功率增益vs.输入功率vs.频率



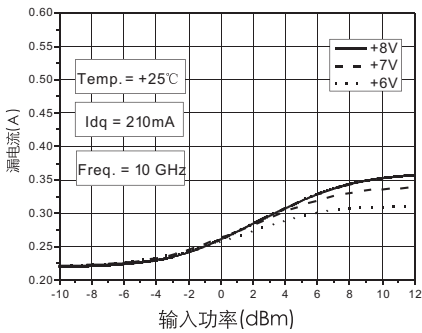
漏电流vs.频率vs.漏电压



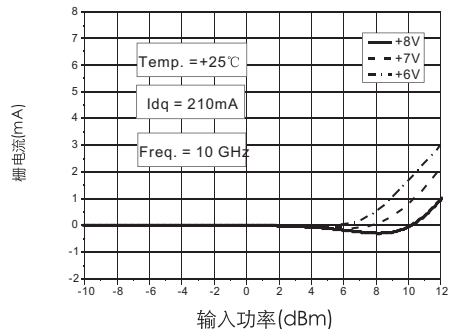
栅电流vs.频率vs.漏电压



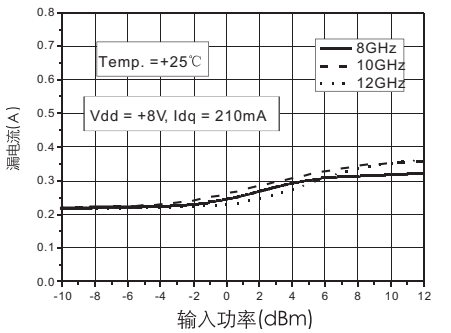
漏电流vs.输入功率vs.漏电压



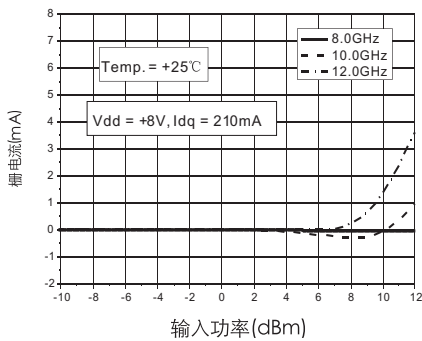
栅电流vs.输入功率vs.漏电压



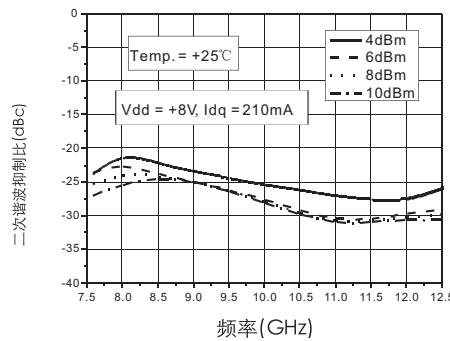
漏电流vs.输入功率vs.频率



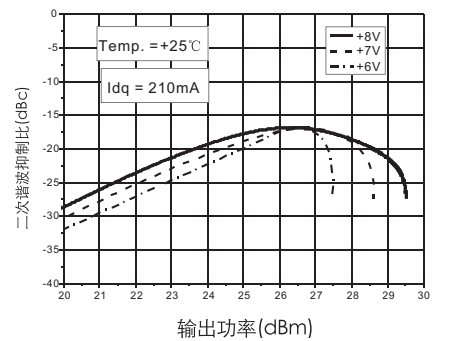
栅电流vs.输入功率vs.频率



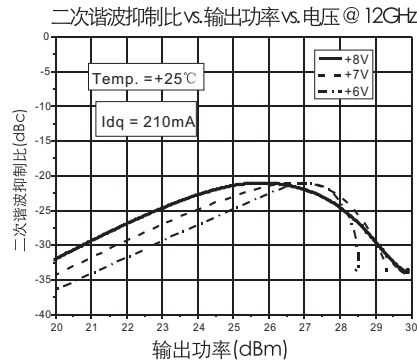
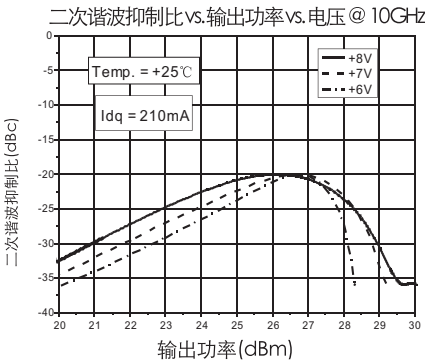
二次谐波抑制比vs.频率vs.输入功率



二次谐波抑制比vs.输出功率vs.电压 @8GHz



BW222型GaAs单片集成功率放大器



极限参数

参数	数值
输入功率PIN, 50Ω	+17dBm
漏电压Vdd	10V
栅电压Vgg	-1.5~-0.4V
热阻 (Rth)	26°C/W
沟道温度TCH	175°C
烧结温度 (20秒, N2保护)	320°C
储存温度	-55 ~ +150°C
工作温度	-55 ~ +85°C

超过以上条件可能引起芯片永久性损坏。

推荐工作条件

参数	数值
漏电压Vdd	+8V
静态漏电流Idq	210mA
栅电压Vgg	-0.6V(典型值)

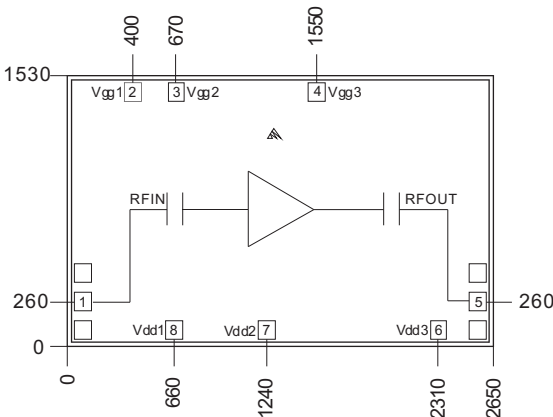


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

键合压点定义

压点编号	功能符号	功能描述	等效电路
1	RFIN	射频信号输入端, 外接50欧姆系统, 无需隔直电容	
6、7、8	Vdd	放大器漏极偏压, 需外置100pF和4.7uF旁路电容	
2、3、4	Vgg	放大器栅极偏压, 需外置100pF和4.7uF旁路电容	
5	RFOUT	射频信号输出端, 外接50欧姆系统, 无需隔直电容	
芯片底部	GND	芯片底部与射频及直流地需要良好接触	

外形尺寸



说明:

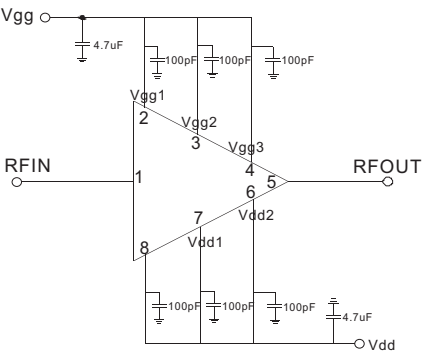
- 单位: 微米
- 芯片背面镀金
- 芯片背面接地
- 键合压点镀金, 1~8压点尺寸: 100umx100um
- 不能在通孔上进行键合
- 外形尺寸公差: ±50um

应用信息

应用电路

- 上电顺序
- 设置Idq最大值为0.5A,
 - 栅电压加-2V
 - 漏电压加+8V
 - 调整栅电压, 使Idq = 210mA (此时Vgg 约为 -0.6V)
 - 加RF输入信号

- 去电顺序
- 关闭RF输入信号
 - 栅电压降至-2V, 确保Idq 接近0mA
 - 设置漏电压Vdd值为0V
 - 关闭漏电压Vdd
 - 关闭栅电压Vgg



● 装配示意图

(滤波电容要离芯片压点尽量近, 尽量减小键合线长度影响)

